

Abstract of the Disclosure:

A test circuit is integrated in a ferroelectric memory component in order to make analog measurements of bit line signals of ferroelectric memory cells. The test circuit, when 5 in a test mode, reads out analog signal values for the respective memory content of the cells and feeds the analog signal values to a downstream evaluation device. The test circuit is integrated as an analog circuit in the ferroelectric memory component and, in the test mode with non-10 activated or disconnected sense amplifiers, is configured to output analog bit line signals from the memory component to a point outside the memory component.

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